REMARKS

Applicant thanks the Examiner for the telephone interview dated August 31, 2009, in which claims 1, 21, 22, and the Edwards and Kimura references were discussed. An agreement was reached that the Kimura's two data drive circuit configuration is not compatible with the digital to analog conversion circuit of Edwards, and that a person of ordinary skill in the art would not have combined the Kimura and Edwards references.

The comments of the Applicant below are each preceded by related comments of the Examiner in the Office Action dated June 1, 2009 (in small, bold type).

As to claim 1, Edward teaches an active matrix display (i.e. the TFT LCD) device comprising a row and column array of picture elements (see Fig. I),

sets of row and column address conductors for selecting rows of picture elements and providing data signals to the picture elements of a selected row respectively (i.e. the column and row electrode that lead to the individual LC pixel) (see Fig. I),

drive means for supplying selection signals and multi-bit digital data signals respectively to the set of row address conductors and the set of column address conductors (see Fig. I, elements 21, 23, and 25), and

in which the multi-bit digital data signals supplied to the column address conductors are converted into analogue voltage levels for use by the picture elements by a plurality of serial charge redistribution digital to analogue conversion means (see Fig. 3, [0023-0024]),

each conversion means comprising at least first and second capacitances interconnectable by at least one conversion switch and between which charge is shared (see Fig. 3), and

in which the first and second capacitances of a conversion means are provided by the capacitances of two column address conductors (see Fig. 7, 19a, 19b),

however, Edward is silent the drive means is arranged to alternate the supply of data signals to the first and second column address conductors.

Kimura teaches to alternate the supply of data signals to the first and second column address conductor (i.e. Kimura teaches the alternating data line input to the LCD active matrix) (see Fig. 4, Col. 3, Lines 7-35).

Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to have used the alternating data line design of Kimura in the Edward's LCD system in order to implement an inversion system to reduce flickering of the display (see Kimura Col. 3, Lines 63-67).

Claim 1

Claim 1 would not have been obvious in view of Edwards and Kimura because there is no reason to combine the two references. Applicant disagrees with the Examiner's assertion that using the alternating data line design of Kimura in Edwards' LCD system would reduce flickering of the display. Applicant contends that, applying the alternating data line design of Kimura in Edwards' LCD system would render Edwards' system unsuitable for its intended purpose.

Edwards discloses using the column electrode capacitance as part of the digital to analogue conversion circuit by dividing columns into separate sections and serially performing the conversion via switching elements (abstract). In one example shown in FIG. 3 of Edwards, a column drive circuit 25 applies a voltage to the column electrode, representing the state of the least significant bit of the digital data to be converted, so that a charge corresponding to the least significant bit of the digital data is transferred to the upper half of the column electrode and the lower half of the column electrode is charged to a predetermined voltage, e.g., earth potential. Charge sharing then takes place between the two halves of the column capacitance and the voltages on the capacitors equalize. A voltage representing the next bit of the digital data is generated at the output amplifier 33 of the column drive circuit 25, and this second bit is transferred to the upper half of the column electrode. Then charge sharing takes place between the two components of the column capacitance. This process is repeated for each bit of the digital data in turn. See FIGS. 3 and 4 and paragraph [025] of Edwards. Edwards discloses another example in FIG. 7, and indicates that the conversion process used in the circuit of FIG. 7 is similar to that described in FIGS. 3 and 4 (paragraph [0028]).

Kimura discloses using a first data drive circuit 2 to drive a first address conductor Dm using a first data signal VDm and a second data drive circuit 3 to drive a second address conductor Dm+1 using a second data signal VDm+1, in which the polarity of the first data signal VDm is opposite to the polarity of the second data signal VDm+1. Kimura discloses that, synchronously with the application of a gate signal, a first data signal VDm (FIG. 5b) from a first data drive circuit 2 and a second data signal VDm+1 (FIG. 5c) from a second data drive circuit 3 are applied to odd and even numbered column conductors, respectively. Thus, in Kimura, the

data signals VDm and VDm+1 are applied by two data drive circuits to two column conductors at the same time, and the signals VDm and VDm+1 have opposite polarity. Kimura states that by shifting the phase of the signal between the adjacent pixels such that they have opposite polarities, screen flicker can be reduced (col. 4, lines 19-24).

There are at least two reasons that a person of ordinary skill in the art would not have applied Kimura's driving technique to the digital-to-analog conversion circuit of Edwards.

Reason 1:

It is unclear how Kimura's two data drive circuits can be applied to Edwards' conversion circuit. Suppose a multi-bit digital signal is to be converted to an analog signal using the circuit shown in FIG. 7 of Edwards. The multiple bits of the digital signal are sequentially output from the output amplifier 33 to the column electrode 19a, in which charge sharing between column electrodes 19a and 19b takes place after each bit is provided to the column electrode 19a. Kimura discloses using two data drive circuits to synchronously drive adjacent address conductors. It is unclear how someone of ordinary skill in that art can use Kimura's two data drive circuits to synchronously drive the two column electrodes 19a and 19b in order to convert a multi-bit digital signal into an analog signal. It seems necessary to split the multi-bit digital signal into two parts, so that some bits of the multi-bit digital signal are provided by the first one of Kimura's data drive circuit, and other bits of the multi-bit digital signal are provided by the second one of Kimura's data drive circuit. However, such splitting of a multi-bit digital signal among two data drive circuits is neither disclosed nor suggested in Edwards or Kimura.

Reason 2:

It is unclear how Kiumra's data signals having opposite polarities can be applied to Edwards' conversion circuit. Kimura discloses that the first data signal VDm used to drive the first address conductor Dm and the second data signal VDm+1 used to drive the second address conductor Dm+1 have opposite polarities (col. 3, lines 17-19), and that using data signals having opposite polarities has the advantage of reducing flicker (col. 4, lines 19-24). In Edwards'

circuit, charge sharing takes place between column electrodes 19a and 19b after each bit is provided to the column electrode 19a, and the accumulated charge on the electrodes 19a and 19b at the end of the conversion process represents the converted analog signal. If Kimura's first and second data drive circuits provide data signals that have opposite polarities to Edwards' column electrodes 19a and 19b, charge sharing of the signals between column electrodes 19a and 19b would result in errors in the conversion process.

For example, suppose a 4-bit digital signal "1111" is to be converted to an analog signal. In the example of FIG. 7 of Edwards, the four bits of "1" are sequentially provided to the column electrode 19a, and charge sharing takes after each bit is provided to the column electrode 19a. If Kimura's driving technique were to be applied to Edwards' conversion circuit, then "1" "-1" "1" and "-1" would be alternately provided to the column electrodes 19a and 19b, and charge sharing takes place after each bit is provided to the column electrode 19a or 19b. The charges accumulated on the column electrodes 19a and 19b at the end of the conversion process would not be an accurate analog representation of the digital signal "1111".

It is unclear how someone of ordinary skill in that art can use Kimura's two data drive circuits that provide data signals having opposite polarities to drive the two column electrodes 19a and 19b in order to accurately convert multi-bit digital signals into an analog signals. If Kimura's two data drive circuits were to provide data signals having the same polarities, then it would not achieve the advantage alleged by the Examiner of reducing flicker.

MPEP 2143.02 states that a reasonable expectation of success of modifying the prior art is required to support a prima facie obviousness rejection. Applicant notes that in the case of Edwards and Kimura, there is no reasonable expectation that Edwards can be modified according to the teaching of Kimura to use two separate data drive circuits to provide data signals having opposite polarities to drive two column electrodes while still properly performing the function of converting multi-bit digital signals into analog signals.

Claims 12 and 17 are patentable for at least similar reasons as those applied to claim 1.

Claim 21

Edwards and Kimura do not describe and would not have made obvious "a digital data output that is arranged to alternate the supply of data signals to the first and second column address conductors of each conversion means," as recited in claim 21. Edwards discloses a single amplifier 33 and two column conductors 19a and 19b, but the amplifier 33 does not alternate the supply of data signals to the first and second column conductors 19a and 19b.

Kimura discloses that, synchronously with the application of a gate signal, a first data signal VDm (FIG. 5b) from a first data drive circuit 2 and a second data signal VDm+1 (FIG. 5c) from a second data drive circuit 3 are applied to odd and even numbered column conductors, respectively. In Kimura, the data signals VDm and VDm+1 are applied by two data drive circuits to two column conductors at the same time. Thus, Kimura also does not disclose or suggest a digital data output that is arranged to alternate the supply of data signals to the first and second column address conductors.

Claims 23 and 25 are patentable for at least similar reasons as those applied to claim 21.

Claim 22

Edwards and Kimura do not describe and would not have made obvious a drive means that is arranged to alternate in time the supply of data signals to the first and second column address conductors, as recited in claim 22.

Edwards discloses a single amplifier 33 and two column conductors 19a and 19b, but the amplifier 33 does not alternate in time the supply of data signals to the first and second column conductors 19a and 19b.

Kimura discloses that, synchronously with the application of a gate signal, a first data signal VDm (FIG. 5b) from a first data drive circuit 2 and a second data signal VDm+1 (FIG. 5c) from a second data drive circuit 3 are applied to odd and even numbered column conductors, respectively. In Kimura, the data signals VDm and VDm+1 are applied by two data drive

circuits to two column conductors at the same time. Thus, Kimura also does not disclose or suggest drive means that is arranged to alternate in time the supply of data signals to the first and second column address conductors.

Claims 24 and 26 are patentable for at least similar reasons as those applied to claim 22.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply $312 for the excess claim fees and any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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